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REMARKS

Claims 1-34 are in the present application.

Applicants and Applicant's attorney representatives wish to acknowledge with appreciation the telephone interview conducted with Examiner Thuan V. Do on June 3, 2004. Examiner Do was kind enough to discuss the pending claims and the cited references in an effort to advance prosecution of the present application.

Claims 1-4, 7, 10-14, 17, 20-24, 27, and 30 were rejected under 35 USC 103(a) as being unpatentable over Tsai et al., U.S. Pat. No. 5,617,328 (hereinafter Tsai), in view of Chang et al., U.S. Pat. No. 6, 415, 426 (hereinafter Chang). This rejection is traversed.

As discussed in the interview, Applicants respectfully submit that there are significant, fundamental differences between the pending claims and the cited references. The differences are such that the 35 USC 103(a) rejection of claims 1-4, 7, 10-14, 17, 20-24, 27, and 30 are not supported by the disclosure of the cited and relied upon references.

Applicants emphasize that the pending claims relate to and recite designing an integrated circuit (IC) design-specific cell. Applicants' recitation and use of the term "design-specific cell" in the context of automated IC designs is consistent with the specification. The Office is directed to refer to the background section of the specification for a detailed disclosure regarding design-specific cells in the context of automated IC designs.

Moreover, Applicants' recitation and use of the term design-specific cell in the context of automated IC designs is consistent with the commonly understood and accepted use of design-specific cell and standard cell by those of ordinary skill and knowledge in the art of automated IC design.

Tsai is concerned with physical design(i.e., generation of polygon structures drawn on silicon) for some very special classes of circuits that have a highly repetitive physical layout. This is abundantly clear from the Abstract, Background, Summary of Invention and the Detailed Description thereof. Tsai is concerned with optimization at a layout geometry level (i.e., polygonal shapes), not concerned with transistor-level circuit optimization for design-specific (i.e., not highly repetitive) circuits that can constitute a "standard cell" in today's standard cell based ASIC design techniques.

Contrary to the term design-specific cell recited in the claims, the cited and relied upon Tsai (primary reference) discloses "cells" in the context of "integrated circuit layout, design, and fabrication" (See Tsai Abstract). The term "cell" used in Tsai refers to a regularly repeated or ordered physical structure of two-dimensional arrays of storage cells. Each storage cell stores one particular bit of the eight bits data word. (See Tsai, cool. 1, ln. 20-45 and Fig. 1) Clearly, Tsai's disclosed cells are not "design-specific cells" as claimed by Applicants.

Furthermore, Tsai explicitly states that "[D]esign means a geometrical description of the physical locations of components and regions of a layout" (See Tsai, col. 1., ln. 30-31) Thus, it is clear that Tsai relates to IC layout, layout design, and the fabrication of such IC layouts. That is, Tsai discloses a method for generating repetitious patterns in an IC layout. Tsai discloses an method of arranging and placing IC regions and components. (See Tsai, Abstract)

Regarding the alleged teaching of Tsai, it is clear that Tsai does not in fact disclose Applicants' claimed, mapping to a transistor-level representation of the design-specific cell, the mapping based on the design specification, and evaluating the transistor-level representation of the design-specific cell for meeting the design specification, as alleged by the Office Action. Tsai instead discloses an automatic code pattern generator that receives a "plurality of instructions defining the physical layout of regularly repeated or ordered regions

and components." The instructions are disclosed as "defining polygon shapes, their physical layout, and the mapping between addresses and addressed cells associated with each polygon of the layout." (emphasis added) (See Tsai, col. 3, ln. 11-35)

Clearly, Tsai, as cited and relied upon, discloses a code generator that receives layout instructions for polygons, the placement (i.e., layout) of the polygons, and the mapping therebetween. There is no disclosure or suggestion for Applicants' claimed mapping to a transistor-level representation of the design-specific cell, the mapping based on the design specification. The only mapping disclosed by Tsai is the mapping between addresses and ordered repeated regions of the layout of polygons therein. There is no disclosure or suggestion of mapping to a transistor-level representation of the design-specific cell. Tsai only discloses mapping between its so-called (different than Applicants') cells. Tsai does not disclose or suggest any mapping internal (i.e., transistor-level) to a design-specific cell, as claimed by Applicants.

Furthermore, as discussed above, Tsai does not disclose design-specific cells. Instead, Tsai discloses regularly repeated or ordered regions and components.

Also, Tsai does not disclose Applicants' claimed "evaluating the transistor-level representation of the design-specific cell for meeting the design specification", as alleged by the Office Action. Instead, Tsai discloses "the processor 110 generates a code layer including a mapping relationship between addresses and corresponding cells...processor 110 simply generates one or more formulas which the processor 110 can evaluate in determining the correspondence between each cell and it corresponding address" (See Tsai, col. 7, ln. 37-50) Tsai discloses evaluating the correspondence between each cell and it corresponding address. Clearly, Tsai does not disclose or suggest Applicants' claimed evaluating the transistor-level representation of the design-

specific cell for meeting the design specification. At no point in the disclosure thereof does Tsai disclose or suggest (mapping and) evaluating the transistor-level representation of the design-specific cell for meeting the design specification.

Tsai does not disclose or suggest transistor-level representation mapping, transistor-level representation evaluation, and a design-specific cell (only repeated ordered regions and components).

Chang, like Tsai, is related to the arrangement and layout of IC components, not an automated method for designing an integrated circuit (IC) design-specific cell, as claimed by Applicants. Chang is cited and relied upon for allegedly disclosing the use of timing characteristics of a cell in a desgn specification.

As discussed in the telephone interview, Chang discloses an analysis method for the placement of cells in an IC design. Chang discloses a global placement process and software for the global placement of functional cells in an IC design. There is no disclosure or suggestion of a design specification for electrical behavior or transistor-level characteristic of the design-specific cell in Chang since the timing characteristic of Chang relates to "the timing characteristics of the cell" (See Chang, col. 7, ln. 47-49) Since Chang is concerned with the global placement of the cell, Chang accordingly discloses the timing characteristics of the cell, not transistor-level design specifications. The design specification of Chang is related to the overall global characteristics of the cell, not a design specification for electrical behavior or transistor-level (i.e., within the cell) characteristic of the design-specific cell, as claimed by Applicants.

Claim 11, reciting a system for automatically designing an IC design-specific cell, claim 21, reciting a design-specific cell produced by an automated IC design process, and claim 30, reciting a computer storage medium, are each

worded similar to claim 1 to clearly state that the claimed design specification relates the electrical behavior or transistor-lev l characteristics of the design-specific cell of the IC being designed.

Again, the design specification disclosed by Tsai is related solely to the physical layout of regularly repeated or ordered regions and components on one or more layers of an IC chip. (Tsai, col. 3, ln. 24-27). Thus, it is clear that Tsai is clearly and only directed to the physical layout of the repeated patterns in an IC design, not the electrical behavior or transistor-level characteristics of the design specification as claimed by Applicants.

Therefore, even if the cell timing characteristic disclosure of Chang were incorporated into Tsai, it is not seen where the disclosure or suggestion for Applicants' claimed method (claim 1), system (claim 11), design-specific cell (claim 21), and storage medium (claim 30) is established or supported (i.e., proper) by the Office Action's asserted combination of Tsai and Chang. Clearly, Applicants claim a method, system, design-specific cell, and storage medium including the design specification for the electrical behavior or transistor-level characteristics for the design-specific cell.

Accordingly, Applicants respectfully submit that claim 1, and similarly worded claims 11, 21, and 30, are patentable over Tsai and Morgan under 35 USC 103(a). Therefore, the reconsideration and allowance of claims 1, 11, 21, and 30 is earnestly solicited.

Claims 2-4, 7, and 10 depend from claim 1. Applicants respectfully submit that claims 2-4, 7, and 10 are patentable over Tsai and Morgan under 35 USC 103(a) for at least the reasons stated above regarding claim 1.

Claims 12-14, 17, and 20 depend from claim 11. Applicants respectfully submit that claims 12-14, 17, and 20 are patentable over Tsai and Morgan under

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Claims 2-4, 7, and 10 depend from claim 1. Applicants respectfully submit that claims 2-4, 7, and 10 are patentable over Tsai and Morgan under 35 USC 103(a) for at least the reasons stated above regarding claim 1.

Claims 12-14, 17, and 20 depend from claim 11. Applicants respectfully submit that claims 12-14, 17, and 20 are patentable over Tsai and Morgan under 35 USC 103(a) for at least the reasons stated above regarding claim 1.

Claims 22-24 and 27 depend from claim 21. Applicants respectfully submit that claims 22-24 and 27 are patentable over Tsai and Morgan under 35 USC 103(a) for at least the reasons stated above regarding claim 1.

Applicants acknowledge with appreciation the Office Action's indication of allowable subject matter regarding claims 5, 6, 8, 9, 15, 16, 18, 19, 25, 26, 28, and 29 if rewritten in independent form including the limitations of the base and any intervening claims.

In summary, it is respectfully submitted for the reasons set forth above, that this amendment places the application in condition for allowance. Accordingly, it is respectfully requested that claims 1-34 be allowed and the application be passed to issue.

Respectfully Submitted,

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